21.5 A 10b 100MS/s 1.13mW SAR ADC with Binary-Scaled Error Compensation

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In recent years, due to the improvements in CMOS technologies, medium resolution (8 to 10b) SAR ADCs have been able to achieve sampling rates of several tens of MS/s with excellent power efficiency and small area [1]-[4]. When the sampling rate increases, the SAR ADCs suffer from settling issues. In a typical 10b 100MS/s ADC, when the sampling settling time, comparator active time and SAR logic delay are subtracted from each period, the DAC settling time has to be less than 0.4ns in each bit cycle. Such a short time interval is not sufficient for the capacitive DAC to stabilize because the increasing interconnect line impedance in advanced processes slows down the charge transfer, especially in the longest routing path of the DAC capacitor network. Furthermore, the reference voltage sinks noise and line coupling also affects the settling. A non-binary SAR can tolerate DAC settling error at the cost of increased design complexity and hardware overhead [1]. This paper reports a 10b SAR ADC that uses binary-scaled DAC networks for settling error compensation. The ADC achieves 100MS/s while consuming only 1.13mW.

For a conventional binary SAR ADC, if a termination capacitor with the same value as the LSB capacitor is added, the capacitance of the MSB capacitor would be equal to that of the sum of all LSB capacitors. Likewise, the capacitor MSB-1 is equal to the sum of all the remaining LSB capacitors. After each DAC switching, the effective input range is reduced by a factor of 2 as depicted in Fig. 21.5.1. In a typical SAR ADC conversion, the difference between input and reference is less than one LSB in the last cycle. If a wrong decision is made before the last cycle, even if the remaining decisions and their corresponding DAC switching are all correct, the difference between the input and reference in the last cycle is still larger than one LSB, resulting in performance degradation. In a non-binary SAR ADC [1], the input range is reduced by a factor smaller than 2 per each bit cycle. In this case, more decision levels are generated than the conventional design. Different digital codes can represent the same input voltage, meaning different switching procedures can lead to the same result. Hence, a certain range of DAC settling error does not affect the conversion result. However, the non-binary architecture needs extra hardware including control circuits, a ROM to store the bit weights and an arithmetical unit to calculate the sum. Moreover, the non-binary scaled bit weight is not favored for layout matching, which limits the linearity of the DAC network. Unlike a non-binary one, the input range of this work is reduced by a factor of 2. The basic difference of this ADC with the conventional one is that it uses a compensation technique instead of redundancy for tolerating DAC settling error. In some conversion cycles of the presented work, the input range does not reduce but it shifts to compensate for the DAC error (as shown in Fig. 21.5.1).

The DAC switching network in [4] saves 81% in switching energy and 50% in capacitance as compared to the conventional one. Figure 21.5.2 depicts the proposed binary-scaled error compensation SAR ADC where we inserts three compensative capacitors (C_{3C}, C_{6C}, C_{9C}) and a digital error correction (DEC) logic circuit to perform the error compensation. When conversion starts, the input signals are sampled onto the top plates of the two capacitor arrays. Then, the comparator performs the first comparison. Without the three compensative capacitors, the voltage difference of the two DACs will add or subtract $V/2$, depending on the first comparison, where V is the maximum input amplitude. If the comparator makes the second decision at the moment the first DAC switching settles to 50% of its target value ($V/2\times1/2^1$), the maximum error is $V/2$ ($V/2\times1/2^1+V/4$), i.e., the incomplete settling value of the first DAC switching plus the second DAC switching. Because the maximum sum of the remaining voltage values is $V/4$ ($V/8+V/16+\ldots$), a voltage of $V/4$ must be added to compensate for the error. If the comparator makes the second decision after the DAC settles to 75% of its target value, the maximum error is $3V/8$ ($V/2\times1/2^2+V/4$). A voltage of $V/8$ is required to compensate for the error. Binary-scaled capacitors are inserted in the original DAC network to provide compensative voltage values. In the proposed case, the SAR ADC with three compensative capacitors can tolerate settling error of at least 12.5% in each bit cycle. Note the precise error tolerance range depends on where the wrong decision occurs. The amplitude of the input signal swing is $V_{ref}\times(C_{1to9}/C_{total})$ where V_{ref} is the reference voltage range, C_{1to9} is the total capacitance of C_1 to C_9, C_{total} is the total capacitance including C_{1to9}, the three compensative capacitors and the parasitic capacitance at the comparator input terminal.

Figure 21.5.3 illustrates the digital error correction logic, which converts the 13b redundant codes to 10b binary codes. The bit weights of the 13b redundant codes are 512, 256, 128, 128, 64, 32, 16, 16, 8, 4, 2, 2, 1. The digital output equals to $-(64+8+1)+(512\times B_1+256\times B_2+128\times B_3+128\times B_{3C}+\ldots)$. As shown in Fig. 21.5.3, the digital codes have an offset of 73, and the offset is removed by logic operation. Figure 21.5.3 also shows the logic implementation of digital correction circuit, which consists of 5 inverters, 9 full adders, 1 half adder and 10 multiplexers. The half-adder is used to detect overflow. If the signal swing is over range, overflow occurs and the digital output codes will be set to either 0 or 1023 to keep the function normal.

This ADC uses a dynamic comparator with a p-type input pair. The dynamic comparator does not consume static current and hence is suitable for an energy efficient design. Internal control logic triggered by the global clock and comparator output asynchronously generates internal control clocks, which avoids a high frequency clock generator and makes the sampling rate equal to the clock rate. The sampling phase is around 2ns, and each bit cycle is around 0.6ns.

The prototype is fabricated in a 1P6M 65nm CMOS technology with MOM capacitors. Figure 21.5.7 shows the chip micrograph and zoomed in view of the ADC core which occupies 155×165μm^2. The digital error correction circuit only occupies 18×27μm^2. The unit capacitance is around 3.2fF, and the total sampling capacitance of a single capacitor array is 1.86pF. Figure 21.5.4 illustrates the measured static performance (at 100MS/s and 1.2V supply). The peak DNL and INL are 0.58/-0.53LSB and 0.69/-0.61LSB, respectively. Figure 21.5.5 plots the measured SFDR and SNDR versus the input frequency. At 1MHz input frequency, the measured SNDR and SFDR are 59.0dB and 76.5dB, respectively. The resultant ENOB is 9.51b. When the input frequency is up to 50MHz (Nyquist frequency), the measured SNDR and SFDR are 56.0dB and 66.9dB, respectively. Figure 21.2.5 also provides the FFT spectrum of the output signal when the input frequency is close to 10MHz. The analog circuits (the S/H circuit and comparator) consume 0.37mW. The SAR control logic and digital error correction circuits draw 0.46mW. The power consumption of the DAC reference voltage is 0.30mW. Excluding the output buffers, the total power consumption of the active circuits is 1.13mW. Figure 21.5.6 summarizes the performance and the comparison with the state-of-the-art ADCs [2-5]. According to the well-known FOM equation defined as $Power/(2^{ENOB}\times\min\{f_s, 2ERBW\})$, this ADC achieves 15.5fJ/conversion-step, more than 3 times improvement than previous state-of-the-art ADCs. The ADC consumes 1mW while providing more than 9b ENOB and operating at 100MS/s.

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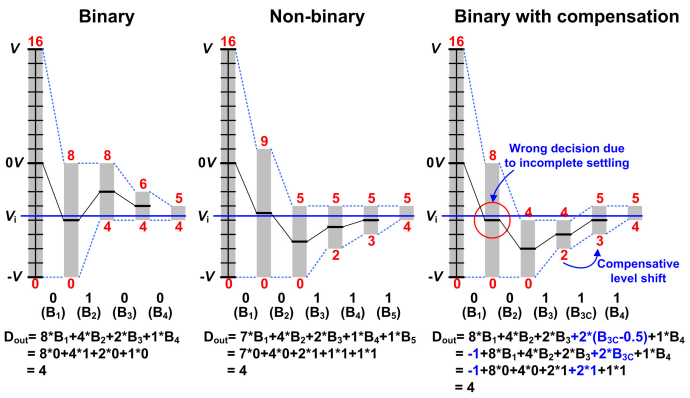

Figure 21.5.1: Successive approximations and digital outputs of different methods.

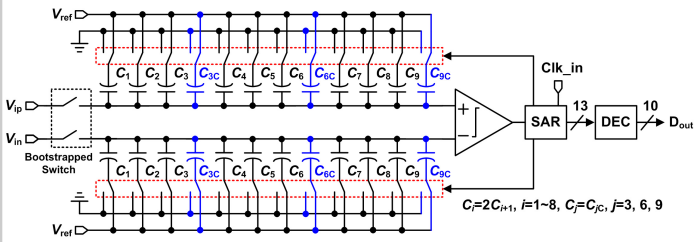

Figure 21.5.2: Block diagram of a 10b SAR ADC with binary-scaled error compensation.

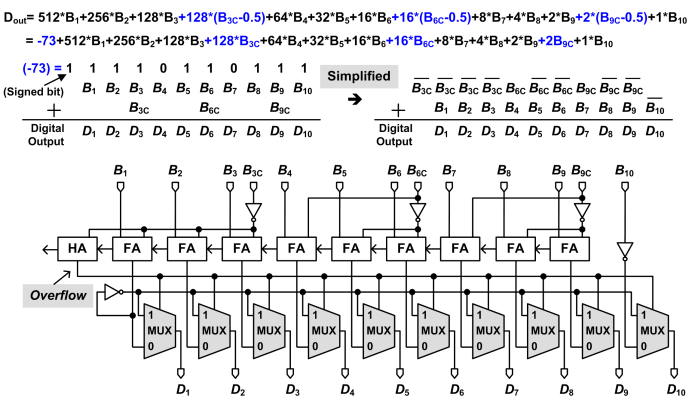

Figure 21.5.3: Digital error correction logic and its implementation.

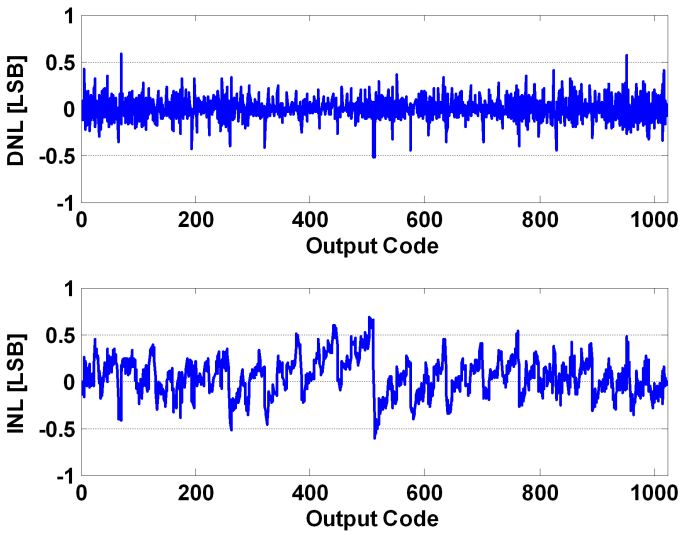

Figure 21.5.4: Measured DNL and INL.

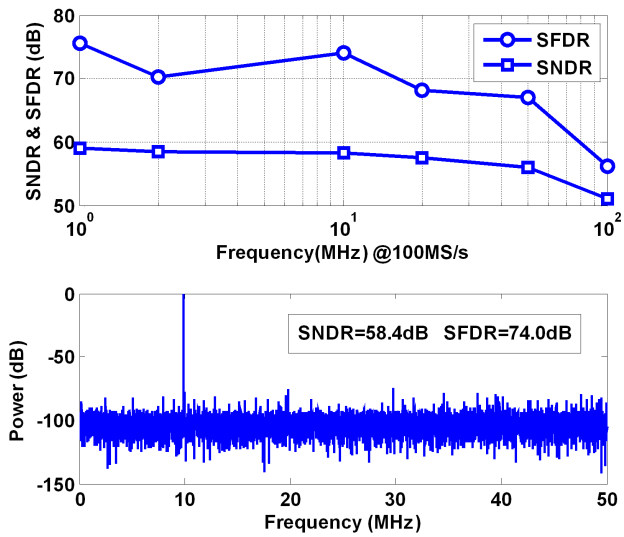

Figure 21.5.5: Measured SFDR and SNDR versus input frequency and 32768-point output FFT spectrum with input frequency close to 10MHz.

Specifications	ISSCC'07 [2]	ISSCC'08 [3]	VLSI'09 [4]	ISSCC'08 [5]	This Work
Architecture	SAR	SAR	SAR	Pipelined	SAR
Technology (nm)	90	90	130	65	65
Supply Voltage (V)	1	1	1.2	1.2	1.2
Sampling Rate (MS/s)	50	40	50	100	100
Resolution (bit)	9	9	10	10	10
ENOB (bit)	7.8	8.56	8.48	9.5	9.51
Power (mW)	0.7	0.82	0.92	4.5	1.13
FOM (fJ/Conv.-step)	65	54	52	62	15.5
Active Area (mm^2)	0.08	0.09	0.075	0.07	0.026

Figure 21.5.6: Performance summary and comparison with the state-of-the-art ADCs.

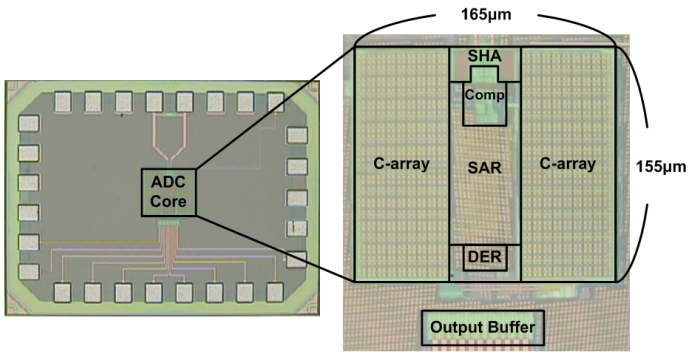

Figure 21.5.7: Chip micrograph and zoomed view.

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