temperature variation, and clamp VVDD close to a target level at runtime in spite of any given NBTI degradation and/or temperature variation within the specified ranges. As a result, active leakage power is reduced by 8%–10%, while dynamic power is reduced by 2.8%–3.7% for the given range of average die temperatures in early chip lifetime. Finally, we demonstrated that they maintain VVDD close to a target level even in the presence of WID spatial process and temperature variations. VVDD clamping helps to improve gate-oxide reliability. Oxide failure rate is reduced by 5% for the fast process corner and ∼4% for the nominal and slow corners at $t = 7.5$ years.

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10-bit 30-MS/s SAR ADC Using a Switchback Switching Method

Guan-Ying Huang, Soon-Jyh Chang, Chun-Cheng Liu, and Ying-Zu Lin

***Abstract*— This brief presents a 10-bit 30-MS/s successive-approximation-register analog-to-digital converter (ADC) that uses a power efficient switchback switching method. With respect to the monotonic switching method, the input common-mode voltage variation reduces which improves the dynamic offset and the parasitic capacitance variation of the comparator. The proposed switchback switching method does not consume any power at the first digital-to-analog converter switching, which can reduce the power consumption and design effort of the reference buffer. The prototype was fabricated in a 90-nm 1P9M CMOS technology. At 1-V supply and 30 MS/s, the ADC achieves an sequenced neighbor double reservation of 56.89 dB and consumes 0.98 mW, resulting in a figure-of-merit (FOM) of 57 fJ/conversion-step. The ADC core occupies an active area of only 190 × 525 μm^2.**

***Index Terms*— Analog-to-digital converter (ADC), energy efficient switching method, low input capacitance, successive approximation, successive-approximation-register (SAR) ADC.**

I. INTRODUCTION

With the feature size of CMOS devices scaled down, the propagation delay of logic circuit decreases significantly. Successive-approximation-register (SAR) analog-to-digital converters (ADCs) have achieved several tens of MS/s to low GS/s sampling rates with 5- to 10-bit resolutions recently [2]–[8]. The comparator and sampling switches are the only analog components of the SAR ADCs, and no building block consumes static power if preamplifiers are not used. Therefore, the SAR ADCs are power- and area-efficient architecture. For some high-conversion-rate applications, power- and area-efficient SAR ADCs possibly replace pipelined ADCs in nanometer-scaled CMOS processes.

In the past few years, several power-efficient switching sequences for the capacitive digital-to-analog converter (DAC) have been proposed. Compared to the conventional switching sequence, the energy-saving [1], monotonic [2], and $V_{\rm cm}$-based [3] switching sequences reduce 69%, 81%, and 90% switching energy, respectively. Although, the $V_{\rm cm}$-based one reduces the most power consumption, it needs more switches and reference voltages than the monotonic one, which increase the complexity and power consumption of the digital control circuits. The monotonic switching sequence has the fewest switches and reference voltages. However, during the conversion process, the common-mode voltage of the comparator input terminal varies from $V_{\rm cm}$ to $V_{{\rm ref}n}$, as shown in Fig. 1(a). It induces dynamic offset and the parasitic capacitance variation of the comparator to affect the ADC linearity.

This brief proposes a SAR ADC using a switchback switching method, which has the fewest number of switches and reference voltage as the monotonic. Moreover, the proposed switching sequence

Manuscript received October 9, 2011; revised January 30, 2012; accepted February 16, 2012. Date of publication March 22, 2012; date of current version February 20, 2013. This work was supported in part by the National Science Council and Himax Technologies Inc., Taiwan, under Grant NSC-98-2221-E-006-156-MY3.

The authors are with the Department of Electrical Engineering, National Cheng Kung University, Tainan 701, Taiwan (e-mail: pet@sscas.ee.ncku.edu.tw; tvlsieic@eecs.northwestern.edu; ckim@korea.ac.kr; soon@mail.ncku.edu.tw).

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Digital Object Identifier 10.1109/TVLSI.2012.2190117

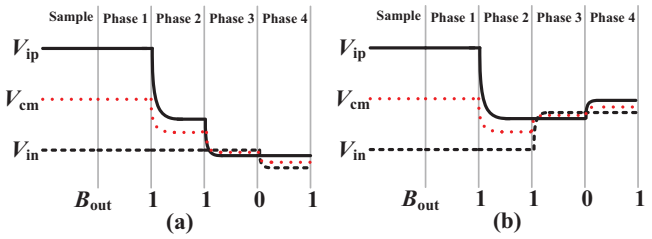

Fig. 1. (a) Waveform of monotonic switching procedure. (b) Waveform of switchback switching procedure.

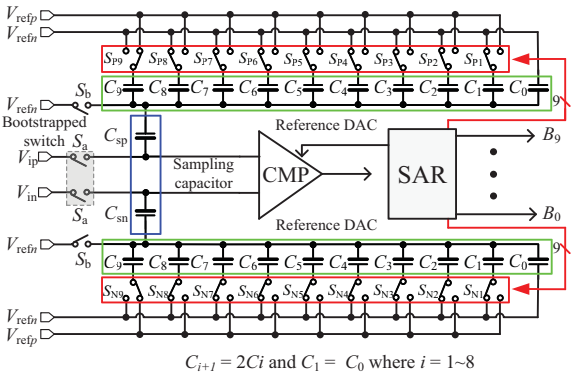

Fig. 2. Block diagram of the proposed ADC.

reduces 50% of the common mode voltage variation, as shown in Fig. 1(b). It does not consume any DAC switching energy at the first switching. Therefore, it can reduce the power consumption and design effort of the reference buffer.

The remainder of this brief is organized as follows. Section II describes the architecture and design concept of the proposed SAR ADC. Section III presents the implementation of key building blocks. Section IV shows the measurement results. Conclusions are given in Section V.

II. Architecture and Design Concept of the Proposed SAR ADC

A. ADC Architecture

Fig. 2 shows the complete block diagram of the proposed ADC [4]. The ADC core consists of two sampling capacitors, two capacitive reference DACs, dynamic-latched comparator and SAR control logic. The proposed capacitive DAC is split into two parts: a reference DAC and a sampling capacitor. The sampling capacitor captures the input signal and the reference DAC provides the reference signal. The reference DAC is a binary-weighted capacitor array which has better linearity than the C-2C capacitor array or the capacitor array with a bridged capacitor.

At the sampling phase, the switches S_a and S_b are turned on and the input signal is sampled onto the sampling capacitors, C_{sp} and C_{sn}. The bottom plate of the most-significant-bit (MSB) capacitor in the reference DAC is switched to V_{refp} and those of LSBs are switched to V_{refn} at the same time. Meanwhile, the reference DAC is at the reset state. Next, the switches S_a and S_b are turned off and the SAR ADC begins the conversion phase. The comparator determines whether V_{ip} is higher than V_{in} or not at the beginning of the conversion phase. If V_{ip} is higher than V_{in}, the MSB will be set to 1. Otherwise, the MSB is 0. Then the MSB triggers the SAR logic to control the reference switching of the DAC by the proposed switchback switching procedure.

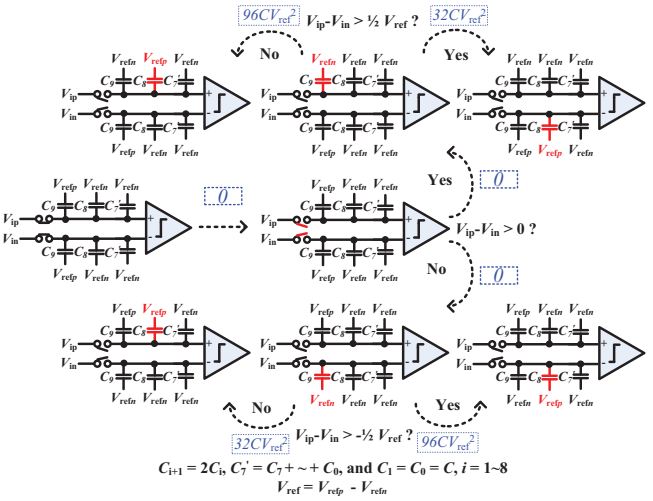

Fig. 3. Switchback switching procedure of 10-bit SAR ADC.

As the monotonic switching procedure, the switchback switching procedure only switches a capacitor in each bit cycle, which reduces both charge transfer in the capacitive DAC network and the transitions of the control circuit and switch buffer, resulting in smaller power dissipation. Moreover, the common-mode voltage of the switchback switching procedure would be downward just for the first switching and then upward for the remainder. Hence, the maximum variation of the common-mode voltage is 1/4 V_{ref} and the common-mode voltage will gradually approach the common-mode voltage of the input signal V_{cm}. It reduces the dynamic offset and the parasitic capacitance variation of the comparator.

Fig. 3 shows an example of the switchback switching method, where a 10-bit binary-weighted capacitive DAC is adopted and it is the same as the reference DAC adopted in Fig. 2. In order to simplify the illustration of the switchback switching method, the sampling capacitor of Fig. 2 is omitted in Fig. 3. The quantitative energy consumption of the first three switching phases is shown. For the switchback switching method, the bottom plate of the MSB capacitor is connected to V_{refp} and the rest are connected to V_{refn} at the sampling phase. Then the sampling switches turn off, the comparator directly performs the first comparison without switching any capacitor. After the MSB is determined, one MSB capacitor will switch to V_{refn}. There is no energy consumption at this conversion step.

For an n-bit SAR ADC, if each digital output code is equiprobable, the average switching energy of the monotonic [2] and V_{cm}-based switching method [3] can be derived as

$$E_{avg,mono} = \sum_{i=1}^{n-1} \left(2^{n-2-i}\right) C V_{ref}^2 \quad (1)$$

$$E_{avg,V_{cm}} = \sum_{i=1}^{n-1} \left(2^{n-2-2i}\right) \left(2^i - 1\right) C V_{ref}^2 \quad (2)$$

where C is the unit capacitance of the DAC and V_{ref} is the reference voltage supply to reference DAC, $V_{ref} = V_{refp} - V_{refn}$. The average switching energy for an n-bit SAR ADC using the switchback switching procedure can be derived as

$$E_{avg,switch} = \sum_{i=1}^{n-2} \left(2^{n-3-i}\right) C V_{ref}^2. \quad (3)$$

For a 10-bit case, the monotonic and V_{cm}-based switching procedures consume 255.5 and 170.2 CV_{ref}^2, respectively, while the

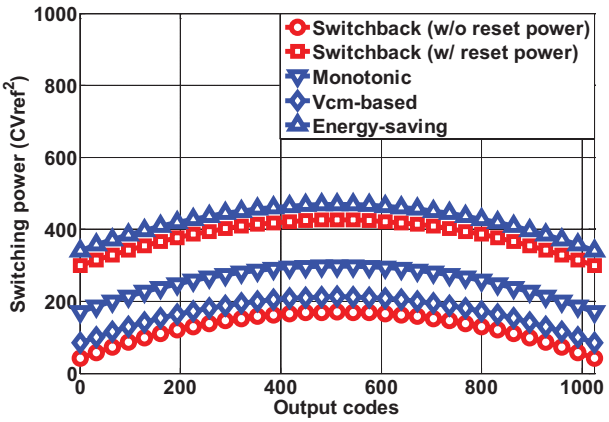

Fig. 4. Switching energy versus output code.

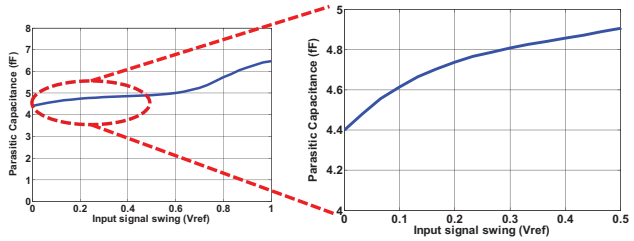

Fig. 5. Parasitic capacitance versus input common-mode voltage at the comparator input terminal.

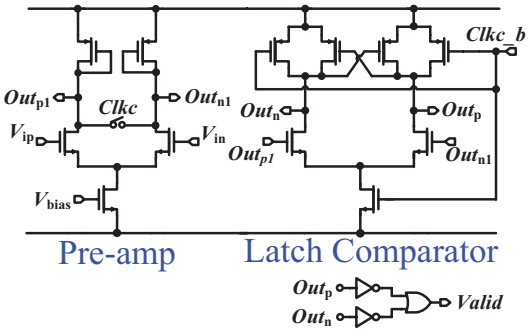

Fig. 6. Dynamic comparator with a pre-amplifier.

proposed switching procedure consumes only 127.5 CV^2_{ref}. The proposed technique thus requires 50% less switching energy than the monotonic one and 25% less than the V_{cm}-based one. Fig. 4 shows a comparison of switching energy for the four methods versus the output code.

Although the switchback switching method consumes less power than the monotonic and V_{cm}-based switching methods during the conversion phase. It must be pre-charged in the sampling phase. For a 10-bit case, if all of the switching methods sample the same input signal, the switchback switching method consumes 255.5 CV^2_{ref}. Fig. 4 also shows a comparison of switching energy for the four methods versus the output code when both sampling and conversion phase are calculated.

Accordingly, the switchback switching method may consume more power than the monotonic and V_{cm}-based switching methods if both sampling and conversion phases are taken into consideration. Nevertheless, it is worth to note that the switchback switching method reduces the design overhead of reference voltage circuit. The reason is for monotonic or V_{cm}-based switching methods, the

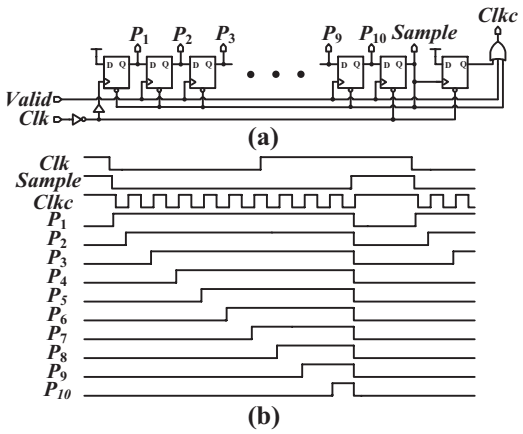

Fig. 7. Proposed asynchronous phase generator. (a) Schematic. (b) Timing diagram.

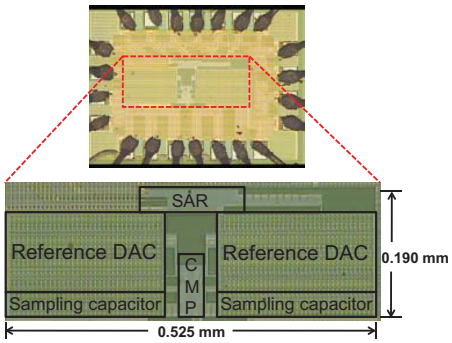

Fig. 8. Die micrograph.

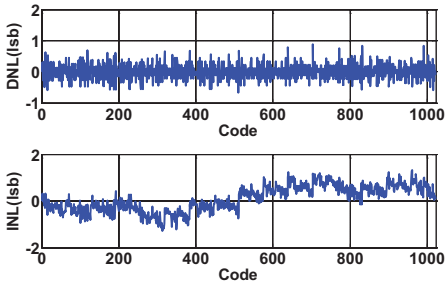

Fig. 9. DNL and INL at 30 MS/s.

MSB capacitor must settle to the reference voltage in a very short time during the conversion phase. The MSB capacitor of switchback switching method is pre-charged in the sampling phase which allows longer settling time than the conversion phase. Therefore, the switchback switching method does not require a fast-settling reference buffer to charge MSB capacitor in the conversion phase.

III. Implementation of Key Building Blocks

A. S/H Circuit

The proposed SAR ADC samples input signal on the sampling capacitors, C_{sp} and C_{sn}, via the bootstrapped switches, S_a and S_b [9].

The nonlinear variation of the parasitic capacitance during the conversion phase, induced by the sampling switch S_a and the comparator input pair, affects the linearity of the proposed SAR ADC. The top-plate parasitic capacitance of the sampling capacitor is a constant value, which does not affect the ADC performance. Fig. 5

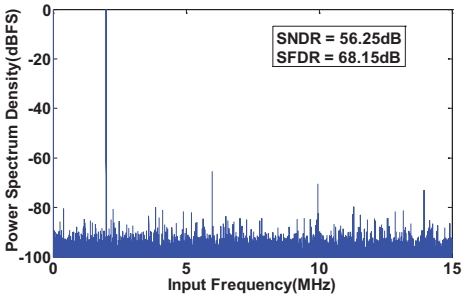

Fig. 10. Measured power spectrum at 30 MS/s and 2-MHz input.

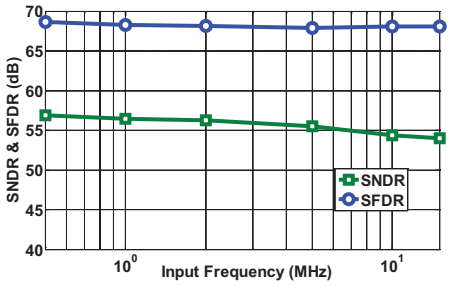

Fig. 11. Dynamic performance versus input frequency.

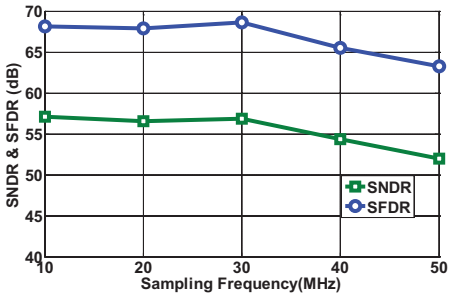

Fig. 12. Dynamic performance versus sampling frequency.

shows the parasitic capacitance at the gate of the comparator input differential pair, $C_{gs} + C_{gd} + C_{gb}$. With the bootstrapped switch, a small-size sampling switch is adopted. During the conversion phase, the bootstrapped switch turns off and the parasitic capacitance of drain terminal, $C_{gd} + C_{ds}$, is smaller than 0.01 fF. Therefore, Fig. 5 just shows the simulated parasitic capacitance of the pre-amp input pair, which is the total capacitance of gate terminal. During the transition of the monotonic switching method, 0–0.5 V_{ref}, where V_{ref} is $V_{refp} - V_{refn}$, the parasitic capacitance varies from 4.4 to 4.9 fF. Moreover, with the switchback switching method, the common-mode-voltage variation decreases from 0.5 to 0.25 V_{ref}. In this case, the parasitic capacitance varies from 4.74 to 4.9 fF.

The voltage of comparator input terminal, V_{CMP}, can be expressed as

$$V_{CMP} = V_{in} + \frac{C_{sp}}{C_{sp} + C_{p1}} V_{DAC} = V_{in} + \left(1 - \frac{C'_{p1}}{C_{total}} - \frac{\Delta C_{p1}}{C_{total}}\right) V_{DAC} \quad (4)$$

where C_{p1} is the parasitic capacitance at the comparator input terminal, including the top-plate parasitic capacitance of the sampling capacitor and the parasitic capacitance of the pre-amplifier. C'_{p1} is the constant part of C_{p1} and ΔC_{p1} is the variable part of C_{p1}. V_{CMP} and V_{DAC} are the voltages of the comparator input and reference DAC output, respectively. V_{DAC} can be written as

$$V_{DAC} = \frac{\sum_{i=1}^{9} Di \cdot 2^{i-1} \cdot C}{\sum_{i=1}^{9} 2^{i-1} \cdot C + \frac{C_{sp} \cdot C_{p1}}{C_{sp} + C_{p1}}} V_{ref}. \quad (5)$$

If the parasitic capacitance C_{p1} is a constant value ($\Delta C_{p1} = 0$), it can be regarded as a fixed gain error and does not affect the dynamic performance. However, C_{p1} here is not a constant value. During the conversion process, ΔC_{p1} is 0.16 fF, which affects the ADC linearity. To achieve 10-bit linearity, assume the maximum error due to ΔC_{p1} must be smaller than 0.5 LSB. From (4), the minimum capacitance of the sampling capacitor C_{sp} is 328 fF. According to (5), the minimum unit capacitance C is 0.64 fF. If the monotonic switching method is adopted, the minimum capacitance of the sampling capacitor C_{sp} is 1025 fF. With the proposed switching method, the minimum input capacitance decrease from 1025 to 328 fF. For routing parasitic capacitance, process variation and matching issues, the adopted values of C_{sp} and C are 400 and 5 fF, respectively. The sampling capacitors and reference DAC are metal-oxide-metal capacitors [2].

B. Dynamic Comparator

Fig. 6 shows the schematic of the comparator which consists of a pre-amplifier and a dynamic latched comparator. With a low sampling capacitance, the kickback noise originated from the latched comparator becomes more critical. Furthermore, the bottom plate of the sampling capacitors, C_{sp} and C_{sn}, are floating and hence sampling capacitors are more sensitive to kickback noise than the conventional case. Therefore, the proposed comparator adopts a pre-amplifier to block the kickback noise and enhance the comparison speed.

TABLE I
SPECIFICATION SUMMARY

Specifications (unit)	Experimental results
Supply voltage (V)	1.0
Input range (V_{pp})	1.2
Active area (mm^2)	0.10
Input capacitance (pF)	0.4
Sampling rate (MS/s)	30
DNL (LSB)	$-0.66 \sim 0.88$
INL (LSB)	$-1.27 \sim 1.32$
ENOB (bit)	9.16 @ 30 MS/s
SNDR/SFDR (dB)	56.89/68.65 (0.5 MHz)
	56.25/68.15 (2 MHz)
ERBW (MHz)	15 @ 30 MS/s
Power (mW)	0.98
FOM (fJ/conv.-step)	57

C. SAR Control Logic

To avoid a high-frequency clock generator and a pulse-width modulator (PWM), the proposed ADC uses an asynchronous control circuit to internally generate the necessary clock signals [5]. Fig. 7 shows a schematic and a timing diagram of the asynchronous phase generator. The conversion process starts once the system clock is switched to low. *Sample* is the sample signal which turns on the sampling switches. After ten comparisons, *Sample* will be set to high to sample the input signal until the system clock, *Clk*, switches to low. Therefore, the duty cycle of the system clock, *Clk*, is 50% and no PWM is needed for the integration application. The dynamic

TABLE II
COMPARISON TO STATE-OF-THE-ART WORKS

Specifications (unit)	JSSC'10 [2]	JSSC'10 [3]	ISSCC'08 [6]	TCAS II'10 [7]	ISSCC'10 [8]	proposed
Architecture	SAR	SAR	SAR	SAR	SAR	SAR
Technology	0.13 mm	90 nm	90 nm	65 nm	65 nm	90 nm
Supply voltage (V)	1.2	1.2	1	1.0	1	1
Sampling rate (MS/s)	50	100	40	80	50	30
Resolution (bit)	10	10	9	9	10	10
Sampling capacitance (pF)	2.5	2.0	5	0.64	0.53	0.4
ENOB (bit)	9.18@0.5 MHz	9.1@1.8 MHz	8.56@1 MHz	8.18@39 MHz	9.16@2 MHz	9.16@0.5 MHz
Power (mW)	0.826	3	0.82	1.7	0.82	0.98
FOM (fJ/conv.-step)	29	55	54	39	30	57
Active area (mm^2)	0.052	0.181	0.09	0.05	0.039	0.1

comparator generates the *Valid* signal after each comparison. *Clkc* is the control signal of the dynamic comparator. P_1 to P_{10} sample the digital output codes of the comparator and serve as control signals for the capacitor arrays to perform the switchback switching procedure.

IV. MEASUREMENT RESULTS

The ADC was fabricated in a 1P9M 90-nm CMOS technology. The micrograph of the ADC core is shown in Fig. 8. The ADC core only occupies an area of 525 × 190 μm. The ADC has a 1.2-V peak-to-peak differential input range. The measurement results of the prototype are presented below.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC are shown in Fig. 9. The peak DNL and INL are $-0.66/0.88$ and $-1.27/1.32$ LSB, respectively.

Fig. 10 shows the measured fast Fourier transform spectrum with an input frequency close to 2 MHz at a 1.0-V supply and a 30-MS/s sampling rate. The measured signal-to-noise distortion ratio (SNDR). and spurious free dynamic range (SFDR) are 56.25 and 68.15 dB, respectively.

Fig. 11 plots the measured SNDR and SFDR versus the input frequency at 30 MS/s. At a low input frequency, the measured SNDR and SFDR are 56.89 and 68.65 dB, respectively. The resultant ENOB is 9.16 bits. When the input frequency increases to 15 MHz, the measured SNDR and SFDR are 53.99 and 68.1 dB, respectively. The effective resolution bandwidth is higher than 15 MHz.

Fig. 12 shows the measured performance versus the sampling frequency with a 0.5-MHz sinusoidal stimulus. When the sampling rate was 10 MS/s, the SNDR and SFDR were 57.13 and 68.17 dB, respectively. When the sampling rate was over 30 MS/s, the performance rapidly degrades because the time for input signal sampling was insufficient.

At a 1.0-V supply and 30 MS/s, the analog part, including the S/H circuit and dynamic comparator, consumes 0.55 mW. The switching power of the reference DAC draws 0.08 mW and the digital control logic consumes 0.35 mW. The pre-amplifier depletes most of the analog power (76%) because it consumes static power consumption. The proposed switching sequence reduces the DAC switching power significantly; it just occupies 8.1% of the total power. Excluding the output buffers, the total power consumption is 0.98 mW. A specification summary of the ADC is listed in Table I.

Table II compares the proposed ADC with other state-of-the-art SAR ADCs [2], [3], [6]–[8]. To compare the proposed ADC to other works with different sampling rates and resolutions, the well-known figure-of-merit (FOM) equation is used

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \min\{2 \times \text{ERBW}, f_s\}}. \quad (6)$$

The FOM of the proposed ADC is 57 fJ/conversion-step at 30 MS/s and a 1.0-V supply. The pre-amplifier consumes 0.46 mW, which makes the FOM larger than the other works. Nevertheless, if the power consumption of the front-end buffer and reference buffer is considered, the FOM of the proposed ADC will be lower than the other works.

V. CONCLUSION

In this brief, a SAR ADC with a new switching method was presented. The proposed switching procedure reduces the parasitic capacitance variation and the comparator dynamic offset induced by input common-mode-voltage variation. The input capacitance of the proposed ADC is just 0.4 pF, which reduces the power consumption and design effort of the front-end buffer. The prototype occupies an active area of 0.1 mm^2, and achieves a 30-MS/s operation speed with power consumption less than 1 mW, resulting in an FOM of 57 fJ/conversion-step.

ACKNOWLEDGMENT

The authors would like to thank National Chip Implementation Center, Hsinchu, Taiwan, for supporting the chip implementation.

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